WHAT IS CLAIMED IS:

1. A microprocessor, comprising:

a trace cache comprising a plurality of trace cache entries, wherein each trace cache entry is configured to store a plurality of operations and a respective plurality of liveness indications, wherein the plurality of operations are generated by at least partially decoding a plurality of instructions;

a trace generator configured to generate the respective plurality of liveness indications for the plurality of operations in each trace cache entry, wherein each liveness indication identifies whether execution of its respective operation depends on a branch operation stored within that trace cache entry.

2. The microprocessor of claim 1, wherein each trace cache entry includes a plurality of operation storage locations each configured to store a single operation, wherein a first portion of the plurality of operation storage locations are dedicated to storage of data operations and a second portion of the plurality of operation storage locations are dedicated to storage of memory operations.

3. The microprocessor of claim 1, further comprising a dispatch unit configured to dispatch operations, wherein the dispatch unit is configured to receive operations and their respective liveness indications from the trace cache, and wherein the dispatch unit is configured to determine whether each operation included in a same trace cache entry is executable dependent on one or more current branch predictions and the liveness indication associated with that operation.

4. The microprocessor of claim 3, wherein the dispatch unit is configured to dispatch each operation included in the same trace cache entry, wherein the dispatch unit is further configured to generate a signal indicating whether each operation is executable dependent

on the liveness indication associated with that operation and the one or more current branch predictions.

5. The microprocessor of claim 4, wherein a scheduler coupled to receive dispatched operations from the dispatch unit is configured to store an indication of whether each dispatched operation is executable, and wherein the scheduler is configured to only issue executable operations to an execution core.

6. The microprocessor of claim 5, wherein in response to a branch operation resolving differently than predicted, the scheduler is configured to update one or more indications associated within one or more operations to indicate that those operations are now executable, wherein the one or more indications previously indicated that the one or more operations were not executable.

7. The microprocessor of claim 3, wherein the dispatch unit is configured to selectively dispatch operations included in the same trace cache entry dependent on whether each operation is executable.

8. The microprocessor of claim 3, further comprising a retire queue, wherein the retire queue is configured to retire operations included in the same trace cache entry in response to all executable operations within the same trace cache entry being ready for retirement.

9. The microprocessor of claim 1, wherein each liveness indication may be specified as one of a plurality of liveness encodings, wherein one liveness encoding indicates that execution of a respective operation is not dependent on any branch operations included within a same trace.

10. The microprocessor of claim 9, wherein another liveness encoding indicates that execution of the respective operation is dependent on a first branch operation included within the same trace.

11. The microprocessor of claim 9, wherein another liveness encoding indicates that execution of the respective operation is dependent on both a first and a second branch operation included within the same trace.

12. The microprocessor of claim 9, wherein another liveness encoding indicates that the respective operation is invalid.

13. The microprocessor of claim 12, wherein an operation storage location whose associated liveness indication indicates that the respective operation is invalid is stored stores additional data for use with another valid operation included in the same trace.

14. The microprocessor of claim 9, wherein operations stored within the same trace cache entry and having a same liveness encoding are not stored in adjacent operation storage locations.

15. A method, comprising:

at least partially decoding a plurality of instructions into a plurality of operations;

storing a trace of operations within a trace cache, wherein the trace of operations includes one or more operations that depend on a branch operation included in the trace of operations, wherein the trace of operations includes at least some of the plurality of operations; and

generating a liveness indication for each operation included in the trace of operations, wherein the liveness indication indicates whether execution of a respective operation depends on the branch operation.

16. The method of claim 15, further comprising fetching the trace of operations from the trace cache and responsively dispatching at least some of the operations included in

the trace of operations, wherein said dispatching comprises determining whether each operation included in the trace is executable dependent on one or more current branch predictions and the liveness indication associated with that operation.

17. The method of claim 16, wherein said dispatching comprises dispatching each operation included in the trace to a scheduler and generating an indication of whether each operation is executable dependent on the liveness indication associated with that operation and the one or more current branch predictions.

18. The method of claim 17, further comprising the scheduler storing the indication of whether each operation is executable; and

the scheduler selectively issuing an operation to an execution core dependent on the indication associated with that operation.

19. The method of claim 18, further comprising the scheduler updating one or more indications associated within one or more operations to indicate that those operations are now executable in response to a branch operation resolving differently than predicted, wherein the one or more indications previously indicated that the one or more operations were not executable.

20. The method of claim 16, wherein said dispatching comprises selectively dispatching operations included in the trace dependent on whether each operation is executable.

21. The method of claim 16, further comprising a retire queue, wherein the retire queue is configured to retire operations included in the trace in response to all executable operations within the trace being ready for retirement.

22. The method of claim 15, wherein each liveness indication may be specified as one of a plurality of liveness encodings, wherein one liveness encoding indicates that

execution of a respective operation is not dependent on any branch operations included within a same trace.

23. The method of claim 22, wherein another liveness encoding indicates that execution of the respective operation is dependent on a first branch operation included within the same trace.

24. The method of claim 22, wherein another liveness encoding indicates that execution of the respective operation is dependent on both a first and a second branch operation included within the same trace.

25. The method of claim 22, wherein another liveness encoding indicates that the respective operation is invalid.

26. A computer system, comprising:

a system memory configured to store a plurality of instructions; and

a microprocessor coupled to the system memory, wherein the microprocessor comprises:

a trace cache comprising a plurality of trace cache entries, wherein each trace cache entry is configured to store a plurality of operations and a respective plurality of liveness indications, wherein the plurality of operations are generated by at least partially decoding the plurality of instructions;

a trace generator configured to generate the respective plurality of liveness indications for the plurality of operations in each trace cache entry, wherein each liveness indication identifies which branch operation

stored within that trace, if any, execution of a respective operation depends on.

27. The computer system of claim 26, wherein each trace cache entry includes a plurality of operation storage locations each configured to store a single operation, wherein a first portion of the plurality of operation storage locations are dedicated to storage of data operations and a second portion of the plurality of operation storage locations are dedicated to storage of memory operations.

28. The computer system of claim 26, further comprising a dispatch unit configured to dispatch operations, wherein the dispatch unit is configured to receive operations and their respective liveness indications from the trace cache, and wherein the dispatch unit is configured to determine whether each operation included in a same trace cache entry is executable dependent on one or more current branch predictions and the liveness indication associated with that operation.

29. The computer system of claim 28, wherein the dispatch unit is configured to dispatch each operation included in the same trace cache entry, wherein the dispatch unit is further configured to generate a signal indicating whether each operation is executable dependent on the liveness indication associated with that operation and the one or more current branch predictions.

30. The computer system of claim 29, wherein a scheduler coupled to receive dispatched operations from the dispatch unit is configured to store an indication of whether each dispatched operation is executable, and wherein the scheduler is configured to only issue executable operations to an execution core.

31. The computer system of claim 30, wherein in response to a branch operation resolving differently than predicted, the scheduler is configured to update one or more indications associated within one or more operations to indicate that those operations are

now executable, wherein the one or more indications previously indicated that the one or more operations were not executable.

32. The computer system of claim 28, wherein the dispatch unit is configured to selectively dispatch operations included in the same trace cache entry dependent on whether each operation is executable.

33. The computer system of claim 28, further comprising a retire queue, wherein the retire queue is configured to retire operations included in the same trace cache entry in response to all executable operations within the same trace cache entry being ready for retirement.

34. The computer system of claim 26, wherein each liveness indication may be specified as one of a plurality of liveness encodings, wherein one liveness encoding indicates that execution of a respective operation is not dependent on any branch operations included within a same trace.

35. The computer system of claim 34, wherein another liveness encoding indicates that execution of the respective operation is dependent on a first branch operation included within the same trace.

36. The computer system of claim 34, wherein another liveness encoding indicates that execution of the respective operation is dependent on both a first and a second branch operation included within the same trace.

37. The computer system of claim 34, wherein another liveness encoding indicates that the respective operation is invalid.

38. The computer system of claim 37, wherein an operation storage location whose associated liveness indication indicates that the respective operation is invalid is stored stores additional data for use with another valid operation included in the same trace.

39. The computer system of claim 34, wherein operations stored within the same trace cache entry and having a same liveness encoding are not stored in adjacent operation storage locations.

40. The computer system of claim 26, wherein if an operation of a certain type is stored within a trace cache entry, the trace generator is configured to not store any operations dependent on that operation within that trace cache entry.

41. A device, comprising:

means for at least partially decoding a plurality of instructions into a plurality of operations;

means for storing a trace of operations, wherein the trace of operations includes one or more operations that depend on a branch operation included in the trace of operations, wherein the trace of operations includes at least some of the plurality of operations; and

means for generating a liveness indication for each operation included in the trace of operations, wherein the liveness indication indicates whether execution of a respective operation depends on the branch operation.

42. A microprocessor, comprising:

a trace cache comprising a plurality of trace cache entries, wherein each trace cache entry is configured to store a plurality of operations and a respective plurality of liveness indications, wherein each liveness indication identifies whether execution of its respective operation depends on a branch operation stored within that trace cache entry;

a dispatch unit configured to receive a trace of operations stored in one of the plurality of trace cache entries from the trace cache, wherein the dispatch unit is configured to handle each operation in the trace dependent on the respective liveness indication associated with that operation.

43. The microprocessor of claim 42, wherein the dispatch unit is configured to use the respective liveness indication associated with each operation in the trace and a branch prediction to determine whether that operation is issuable.

44. The microprocessor of claim 42, wherein the dispatch unit is configured to use the respective liveness indication associated with each operation in the trace to determine which register assignment to use when performing register renaming for that operation.

45. The microprocessor of claim 42, further comprising a trace generator, wherein the trace generator is configured to reduce ordering constraints between operations in the trace having a same liveness indication.

46. The microprocessor of claim 42, wherein the dispatch unit is configured to use the respective liveness indication associated with each operation in the trace to determine whether that operation is issuable in response to detection of a mispredicted branch within the trace.